

Blakely, Sokoloff, Taylor & Zafman LLP (408) 947-820 Title: Method and Agratus For Cache Replacement For A Multiple Variable-Way Associate e Cache (408) 947-8200 Title: Method and A Variable-Way Assoc

e Cache 1st Named Inventor: Salvador Palanca

Application No.: 09/608,507

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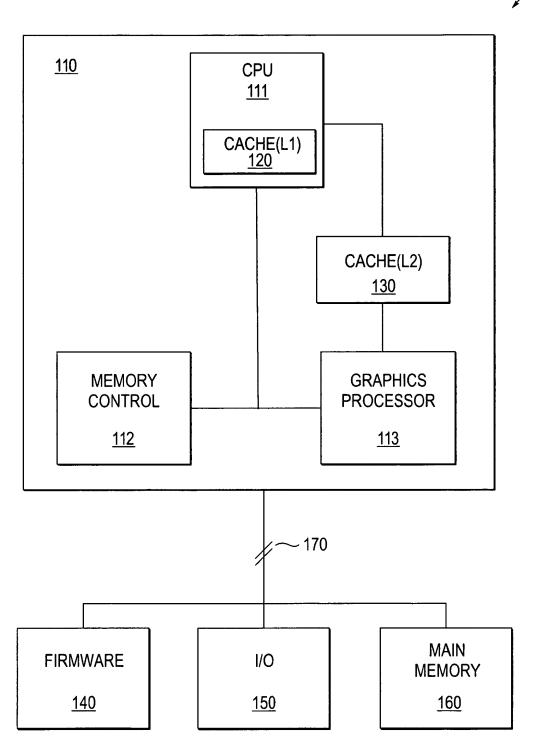


FIG. 1



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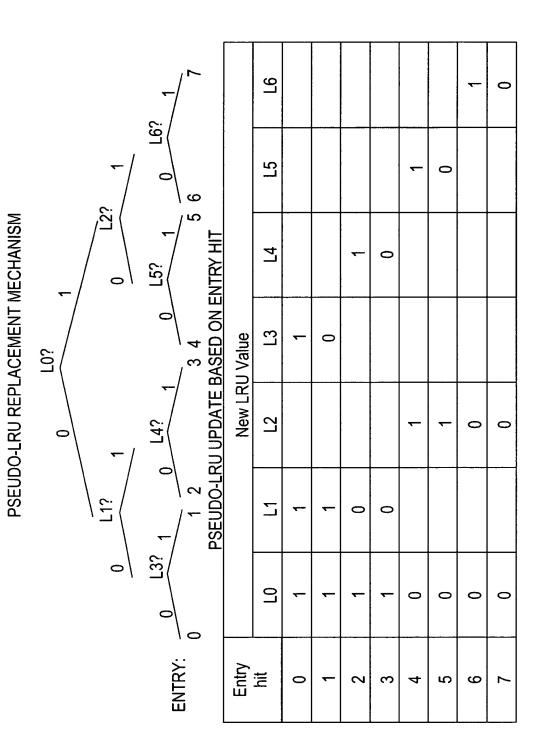
309		310				
0д	1 <sub>A</sub>	0 <sub>B</sub>	1 <sub>B</sub>	<u>311</u>	<u>312</u>	
2 <sub>A</sub>	3 <sub>A</sub>	2 <sub>B</sub>	3 <sub>B</sub>	С	D	
3	<u>313</u>		14	<u>315</u>	<u>316</u>	
E		F		G	Н	
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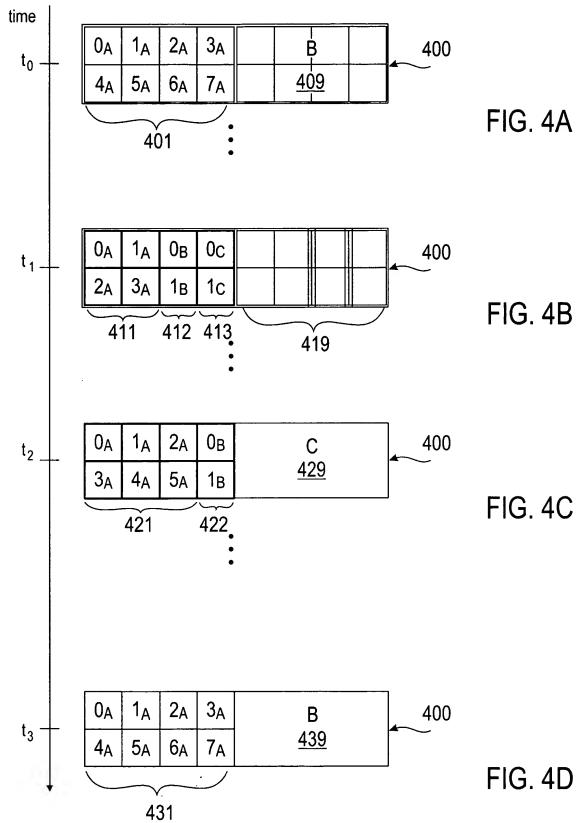


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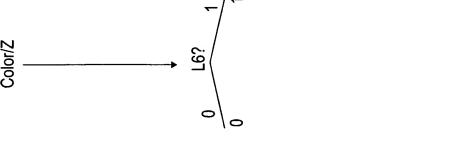
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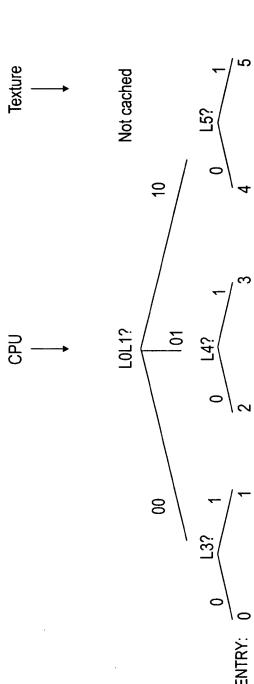
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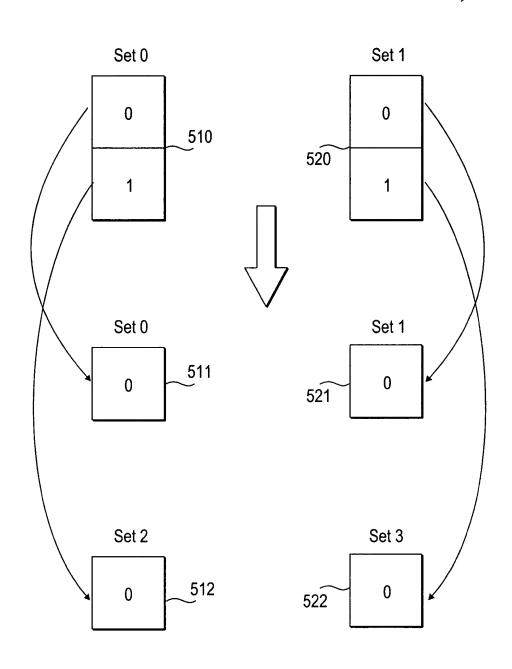


FIG. 6



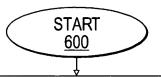
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Take an N-way set associative cache array, where N=(2 to the power M). The cache has L sets, where L=(2 to the power K). The cache line size is H bytes, where H=(2 to the power J). The cache is byte addressable, and the physical address, i.e., PA, is Z bits.

**Physical** PA[Z:0] = tag + set + byte offset = [Z:J+K]+[J+K-1,J]+[J-1,0]address for 620 single access Apply set subdivision to cache implement cache sharing 625

Support two simultaneous accesses in cache sharing mode with configuration 1/2-1/2. The two request types supported are A and B; i.e., CPU and color/Z, with half a cache for each. CPU and color/Z are allocated L/2 sets each.

Number of ways allocated to each request type remains constant; i.e., N-ways.

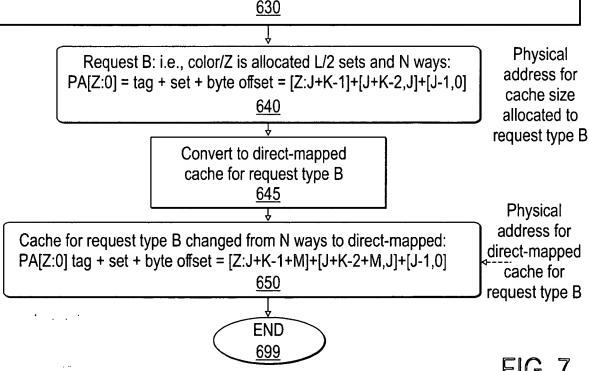
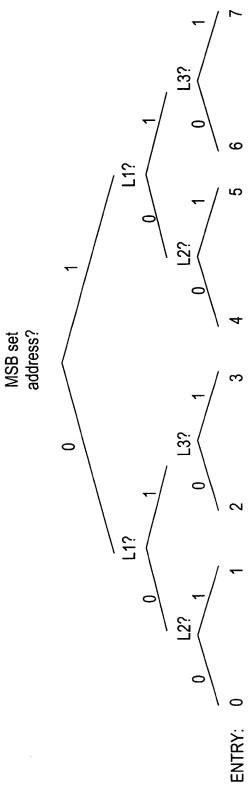


FIG. 7



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PSEUDO-LRU UPDATE BASED ON ENTRY HIT

New LRU value	L3			Į.	0			l	0
	L2	1	0			1	0		
	L1	1	-	0	0	-	1	0	0
	MSB	_	~	_	1	. 0	0	0	0
Entry	hit	0	l	2	3	7	9	9	